I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Sharp Kabushiki Kaisha (Reel/Frame: 012138/0058).

II. RELATED APPEALS AND INTERFERENCES

There are no other prior or pending appeals, interferences or judicial proceedings known to Appellants, the Appellants' legal representative, or the Assignee that are related to, directly affect or will be directly affected by or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF CLAIMS

Claims 1, 2 and 4-40 are pending in the application. Claim 3 has been canceled. Claims 17-40 stand withdrawn from consideration.

Claims 1, 2 and 4-16 stand finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There have been no amendments filed subsequent to final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Applicants' invention relates to a driving arrangement for an active matrix liquid crystal display. The driving arrangement allows the mode of operation of the display, and thus the power consumption and display quality, to be automatically controlled by the *format of the input data itself*. Since the mode of operation is controlled by the

format of the input data itself, Applicants refer to the operation of the driving arrangement of the present invention as being a “content driven format”. (*Emphasis added*; Spec., p. 8, lns. 5-8; and Fig. 9).

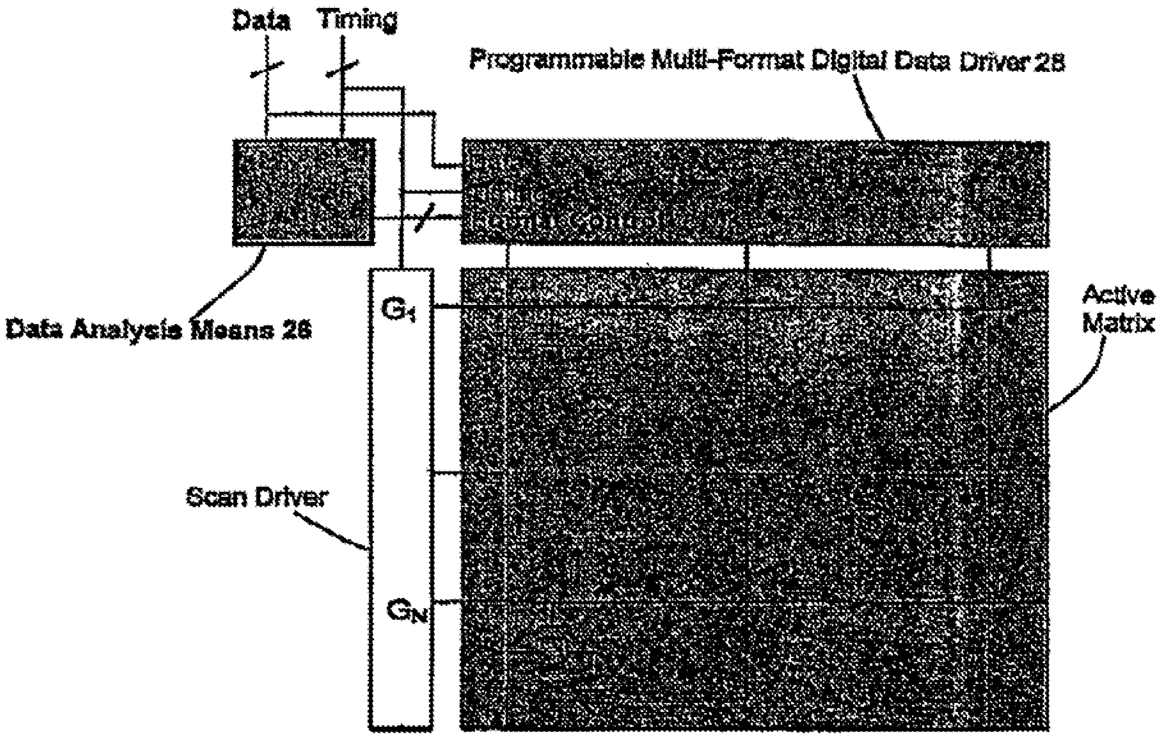


Fig. 9 of Present Application (Present Invention)

Fig. 9 of the present application (reproduced above) exemplifies a driving arrangement in accordance with the present invention. The driving arrangement drives an active matrix liquid crystal display (Active Matrix). The driving arrangement includes a multi-format digital data driver 28 and a data analysis means 26 which provides a 3-bit Format Control signal to the multi-format digital data driver 28 (see multi-bit control line between the data analysis means 26 and the multi-format digital data driver 28).

The multi-format digital data driver 28 is arranged to operate in a plurality of different display modes (e.g., 1-bit per color; m bits per color; n+m bits per color; etc.). For example, Fig. 6 of the present application illustrates how the three-bit Format Control signal (NB, MB, SB) from the data analysis means 26 may control the particular format in which the multi-format digital data driver 28 operates. (Spec., p. 16, ln. 23 - p. 17, ln. 2).

Specifically, the multi-format digital data driver 28 is arranged to receive digital input data in a plurality of different color formats. (See, e.g., Fig. 9 where data is input to both the data analysis means 26 and the multi-format digital data driver 28). The multi-format digital data driver 28 operates in a plurality of different color formats based on the aforementioned Format Control signal received from the data analysis means 26 to drive data lines of the active matrix liquid crystal display to display the input data. (See, e.g., Fig. 9 and lines extending vertically downward from the multi-format digital data driver 28 to the Active Matrix).

The data analysis means 26 receives the input data also, as mentioned above. In accordance with the present invention, the data analysis means 26 determines the color format of the input data (e.g., whether 1-bit per color; m bits per color; n+m bits per color; etc.). The data analysis means 26 in turn controls the multi-format digital data driver 28 to operate in the display mode corresponding to the determined color format of the input data.

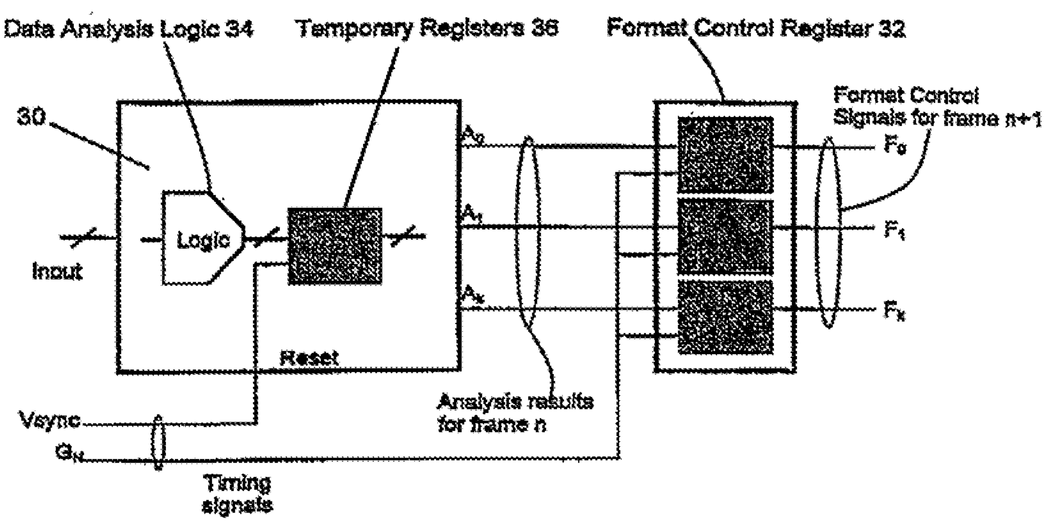


Fig. 10 of Present Application (Present Invention)

For example, Fig. 10 of the present application (reproduced above) illustrates an example of the data analysis means 26 which receives the same input data received by the multi-format digital data driver 28. The data analysis logic 34 and temporary registers 36 analyze the input data itself so as to determine the color format of the input data (e.g., whether 1-bit per color; m bits per color; n+m bits per color; etc.). For each frame of data, the data analysis means 26 outputs the aforementioned Format Control signal to the multi-format digital data driver 28. Referring to Fig. 6 again as an example, if the data analysis means 26 determines that the input data is 1-bit per color input data for a given frame, the data analysis means 26 provides a Format Control signal to the multi-format digital data driver 28 corresponding to “0 0 1".

In the above manner, the multi-format digital data driver 28 is controlled so as to consume less power in low resolution display modes and more power in high resolution display modes based on the determined color format of the input data. (See, e.g., Spec., p. 16, ln. 4 to p. 18, ln. 11).

In summary, the driving arrangement of the present invention allows the mode of operation of the display, and thus the power consumption and display quality, to be

automatically controlled by the _format of the input data itself_. Fig. 10 of the application provides one example of the data analysis means 26 for analyzing the format of the input data itself in order to provide a corresponding Format Control signal to the multi-format digital data driver 28. However, Figs. 14-20 show a variety of alternative embodiments, all of which are considered to fall within the scope of the present invention.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(i) Whether Claims 1, 2, 5, 9, 10 and 12-14 are Unpatentable Under 35 USC §102(e) Based on Nishioka et al.

(ii) Whether Claim 4 is Unpatentable Under 35 USC §103(a) Based on Nishioka et al. in view of Daher.

(iii) Whether Claims 6-8 are Unpatentable Under 35 USC §103(a) Based on Nishioka et al. in view of Koyama et al.

(iv) Whether Claim 11 is Unpatentable under 35 USC §103(a) Based on Nishioka et al. in view of Cairns et al.

(v) Whether Claims 15-16 are Unpatentable Under 35 USC §103(a) Based on Nishioka et al. in view of Misawa et al.

VII. ARGUMENT

(i) Whether Claims 1, 2, 5, 9, 10 and 12-14 are Unpatentable Under 35 USC §102(e) Based on Nishioka et al.

Claim 1 recites a driving arrangement for an active matrix liquid crystal display in which the format control is *content driven*. As is summarized above in Section V, the data analysis means controls the particular display mode of the multi-format digital data driver based on the determined color format of the input data itself. For example, if the input data is high resolution color data, the data analysis means *determines* that the input data is in high resolution color format and *controls* the data driver so as to operate in the high resolution mode. Conversely, if the data analysis means *determines* that the

input data is in low resolution color format, the data analysis means *arranges* the data driver so as to operate in a low resolution mode. In this manner, the invention represents a "*content* driven format control" as noted in Figure 9 of the application. The mode of the multi-format digital data driver is controlled based on a data analysis means that determines the color format of the input data itself.

Appellants have repeatedly argued how the present invention is completely different from the display described in *Nishioka et al.* *Nishioka et al. selects a display mode based on factors which do not include the color format of the input data itself.* Consequently, *Nishioka et al.* does not include a data analysis means as recited in claim 1. That is, *Nishioka et al.* does not teach or suggest a data analysis means which *determines* the color format of the input data and controls the data to operate in the display mode based on the *determined* color format of the input data.

In the absence of any such teaching or suggestion of a driving arrangement having a data analysis means which *determines the color format* of the input data, and controls the data driver to consume less power in low resolution display modes and more power in high resolution display modes *based on the determined color format* of the input data, the rejection of claim 1 is improper and should be withdrawn.

Appellants believe it may be helpful to note that they are in complete agreement with the Examiner that *Nishioka et al.* teaches a display having selectable display modes. Appellants agree that *Nishioka et al.* teaches the control of different display modes involving different frequencies, input data with different numbers of bits, numbers of colors, etc. *However, a fundamental difference between the present invention and Nishioka et al. is how the different display modes are controlled. The driving arrangement of claim 1 utilizes a data analysis means that receives the input data to be displayed and determines the color format of the input data (e.g., whether 1-bit per color; m bits per color; n+m bits per color; etc.). The data analysis means then controls the data driver according to the display mode corresponding to the determined color format. (See, e.g., Fig. 6).*

The Examiner continues, in applicants' opinion, to focus incorrectly on the fact that Nishioka et al. provides a display that operates in different display modes rather than focusing on how Nishioka et al. controls the display so as to operate in different display modes. As applicants have argued previously, Nishioka et al. does not control the display mode based on a determination of the color format of the display input data as recited in claim 1.

FIG.5

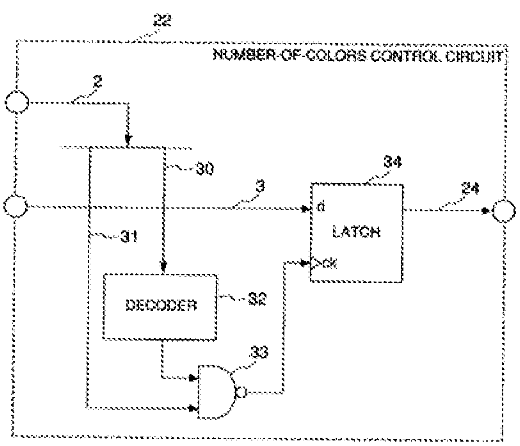


FIG.6

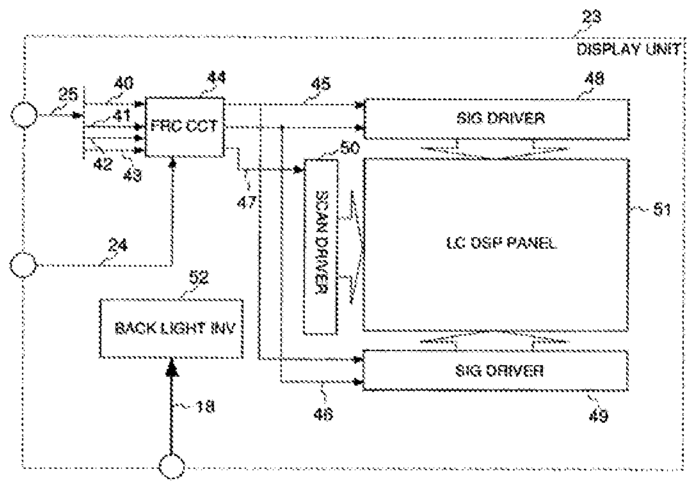


FIG.7

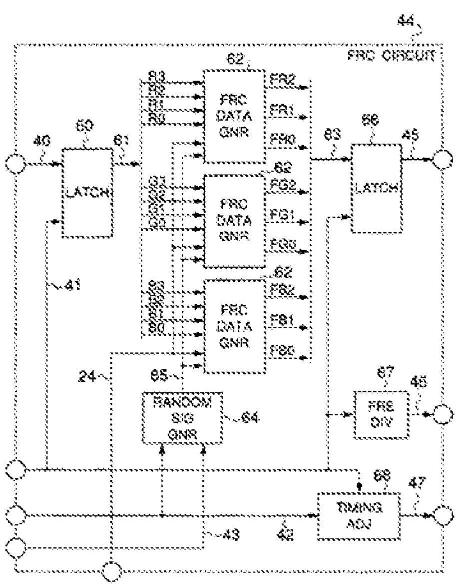
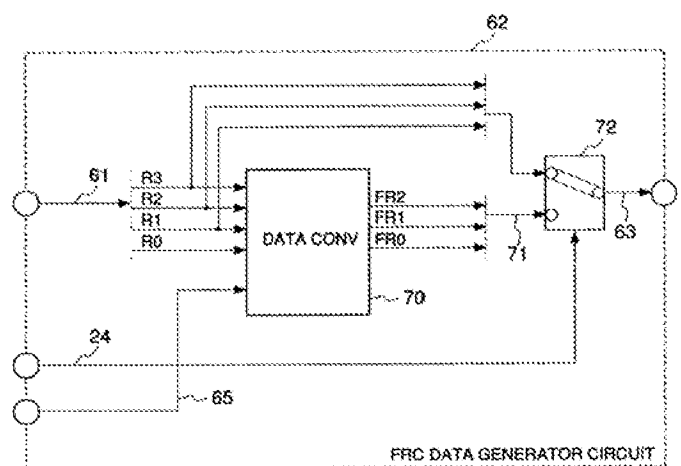


FIG.8



Figs. 5-8 of Nishioka et al.

Figs. 5-8 of *Nishioka et al.* (reproduced above) illustrate the display in relevant part. In maintaining the rejection of claim 1, the Examiner noted in the Advisory action that:

> *Nishioka et al. teach selecting the particular modes (4096, 80Hz mode or 512, 60Hz) based on a data analysis means (44) determination of the color format (4096 or 512) of the input data (24, 25) (see Figures 1, 6-8; Column 4, lines 21-33; Column 8, lines 40-58; Column 9, lines 21-25; Column 13, lines 46-68; Column 14; Column 15, lines 1-39 and final rejection). (Advisory Action, #11).*

The Examiner thus argues that *Nishioka et al.* teaches selecting the particular modes (e.g., 4096, 80HZ mode or 512, 60 HZ mode) based on the determination of the color format of the input data 24, 25 by a data analysis means 44. Stated another way, the Examiner argues that the FRC circuit 44 determines whether the display data is performed at 4096, 80HZ or 512, 60 HZ based on the color format of the input data on lines 24 and 25. Appellants must respectfully disagree for at least the following reasons.

Appellants agree that line 25 in *Nishioka et al.* admittedly includes the display data which is input to the FRC circuit 44 as illustrated in Fig. 6. However, the FRC circuit 44 functions to provide either 4096 or 512 mode data at its output 45 based on the signal input on line 24. (See, e.g., Fig. 6 and Col. 8, lns. 55-58 “This circuit 22 delivers the selection information to the display unit 23 through the signal line 24, and designates the number of colors to-be-developed i.e. 4096 or 512").

More specifically, when the signal input on line 24 is in an “H” state, the FRC frame rate control circuit 44 is instructed that the number of colors to be developed is 512. When the signal input on line 24 is in an “L” state, this indicates to the FRC 44 that the number of colors to be developed is 4096. (column 12, lines 3-11; see Fig. 7.). Whether the signal on line 24 is in an “H” or “L” state depends on whether the CPU 1 writes a “1" or “0" to a latch 34 as illustrated in Fig. 5. In other words, the CPU 1 writes a “1" to the latch 34 when the number of colors to be developed is 512, and writes a “0"

to the latch circuit 34 when the number of colors to be developed is 4096. (see, e.g., column 12, lines 11-14, “the number 512 of the colors can be set when the CPU 1 writes “1" into the allocated address of the latch circuit 34, while the number 4096 can be set when it writes “0"”).

Thus, Appellants respectfully submit that whether the FRC circuit 44 produces 4096 colors or 512 colors depends on whether the CPU 1 writes a “1" or “0" to the FRC circuit 44. Clearly, therefore, the FRC circuit 44 is not acting as a “data analysis means” of claim 1 as argued by the Examiner. The FRC circuit 44 is operating in 4096/80Hz mode or 512/60Hz mode based on the input on line 24. The FRC circuit 44 is not receiving the display input data and determining the color format of the input data as recited in claim 1.

Accordingly, Appellants again repeat that *Nishioka et al.* does not provide control of the different display modes based on a data analysis means that determines the color format of the display input data. The rejection of claim 1 should therefore be reversed and withdrawn.

The Board may be interested to know how or under what circumstances does the CPU 1 in *Nishioka et al.* write a “1" or a “0" to the FRC circuit 44. As Appellants have pointed out in their previous responses, whether the CPU 1 writes a “1" or “0" to the FRC circuit 44 is based on user selection, power source selection, whether the device is in an idle or sleep mode, etc. More specifically, *Nishioka et al.* teaches controlling the particular display mode based on the determination of a user selection (column 9, lines 52-59); a power source (column 10, lines 5-21); and an idle or sleep mode (column 11, lines 40-44). Such means for selection are further emphasized in the claims of *Nishioka et al.* where the claims recite mode selection based on user selection, power source, idle or sleep mode, etc. (See, e.g., claims 3-5, 20 and 22).

Nishioka et al. simply does not teach or suggest that the CPU 1, the FRC circuit 44, or anything else controls the display mode based on analyzing the display input data itself so as to determine the color format of the input data as recited in claim 1.

Appellants therefore again respectfully request reversal and withdrawal of the rejection of claim 1. Claims 2, 5, 9, 10 and 12-14 each depend from claim 1 either directly or indirectly, and therefore are allowable for at least the same reasons.

(ii) Whether Claim 4 is Unpatentable Under 35 USC §103(a) Based on Nishioka et al. in view of Daher.

(iii) Whether Claims 6-8 are Unpatentable Under 35 USC §103(a) Based on Nishioka et al. in view of Koyama et al.

(iv) Whether Claim 11 is Unpatentable under 35 USC §103(a) Based on Nishioka et al. in view of Cairns et al.

(v) Whether Claims 15-16 are Unpatentable Under 35 USC §103(a) Based on Nishioka et al. in view of Misawa et al.

Applicants do not agree with the basis for the rejection for any of grounds (ii) - (v). However, each of the rejected claims depends from claim 1 either directly or indirectly. Thus, these claims may also be distinguished over the teachings of *Nishioka et al.* for at least the same reasons. Furthermore, none of the secondary or tertiary references have been shown to make up for the deficiencies in *Nishioka et al.*

Accordingly, reversal and withdrawal of all of the rejections is respectfully requested.

CONCLUSION

Should a petition for an extension of time be necessary (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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DATE: March 27, 2006

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VIII. CLAIMS APPENDIX

1. A driving arrangement for an active matrix liquid crystal display comprising:

(a) a multi-format digital data driver arranged to operate in a plurality of different display modes, to receive digital input data in a plurality of different color formats, and to drive data lines of the liquid crystal display so as to cause an image to be displayed by the display corresponding to said input data; and

(b) data analysis means arranged to receive said digital input data, to determine the color format of the input data, and to control the data driver to operate in the display mode corresponding to the determined color format of the input data, wherein the data driver is controlled so as to consume less power in low resolution display modes and more power in high resolution display modes based on the determined color format.

2. A driving arrangement as claimed in claim 1, wherein the data analysis means forms part of the data driver.

4. A driving arrangement as claimed in claim 1, wherein said display modes include at least one 1-bit overlay mode.

5. A driving arrangement as claimed in claim 1, wherein the data analysis means analyses each frame of input data in turn, and updates the mode of the data driver at the end of each frame.

6. A driving arrangement as claimed in claim 1, wherein the data analysis means comprises frame comparison means for comparing each frame of input data with the next, and for determining if the input data for a number of consecutive frames is the same.

7. A driving arrangement as claimed in claim 6, wherein the data driver is arranged to operate at more than one refresh rate, and wherein the data analysis means is arranged to control the data driver to operate at a lower refresh rate if the comparison means determines that the input data has remained unchanged for a number of frames.

8. A driving arrangement as claimed in claim 1, wherein the data analysis means comprises a plurality of inputs each arranged to receive a single bit of said digital input data, and wherein at least some of said inputs are connected to a logic OR gate arranged to detect activity on one or more of said at least some inputs.

9. A driving arrangement as claimed in claim 1, wherein the data analysis means is arranged to supply format control signals to the data driver in order to control the display mode of the data driver.

10. A driving arrangement as claimed in claim 9, wherein said format control signals include at least high and low resolution control signals.

11. A driving arrangement as claimed in claim 1, wherein the data driver comprises a plurality of variable bit resolution digital to analogue converters.

12. A driving arrangement as claimed in claim 1, wherein the data driver comprises a plurality of digital data input channels arranged to receive said digital input data.

13. A driving arrangement as claimed in claim 1, wherein the data analysis means comprises a number of storage registers.

14. An active matrix liquid crystal display comprising a driving arrangement as claimed in claim 1.

15. An active matrix liquid crystal display as claimed in claim 14, wherein the driving arrangement is integrated monolithically onto the same substrate as the thin film transistors of the active matrix.

16. An active matrix liquid crystal display as claimed in claim 15, wherein said thin film transistors are poly-silicon

IX. EVIDENCE APPENDIX

No evidence has been submitted by the Appellants or the Examiner.

XI. RELATED PROCEEDINGS APPENDIX

No proceedings have been identified.